An *LLC* Converter Family With Auxiliary Switch for Hold-Up Mode Operation

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***Abstract*—This paper proposed a new half-bridge (HB) *LLC* resonant converter family with pulse-width modulated (PWM) auxiliary switch (sLLC converter) for hold-up mode operation. The proposed sLLC converters could operate with synchronous rectifier, which is suitable for low-output voltage applications. In the proposed converters, an auxiliary switch is added at the primary side to provide charging path for the series resonant inductor. For nominal 400-V input, sLLC achieves same performance as conventional *LLC* converter, and all the good features such as soft switching are naturally retained. For slight input voltage fluctuation, frequency modulation is used to regulate the output voltage. When the input voltage reduces further, HB switches will operate at constant minimum frequency, and the auxiliary switch will operate in the PWM mode to energize the resonant inductor with the bus voltage directly during hold-up period. Thus, the converter achieves higher voltage gain, and the output voltage can be maintained at desired level. To verify the effectiveness of the proposed sLLC converter, operational principle and equivalent circuits will be carefully explained and analyzed in this paper. A 300-W prototype is built for 250–400-V input 12-V output application.**

***Index Terms*—Auxiliary switch, high-voltage gain, hold up, *LLC*, pulse-width modulation (PWM), server power supply.**

I. Introduction

THE power consumption in server and data center field is massive and continuously increasing, due to the rapid growth of computing and internet devices [1], [2]. The typical structure of the front-end ac–dc converter in server and data center power supply is shown in Fig. 1. The PFC stage converts the ac line into 400-V dc, which is further converted to 12 V by the dc–dc stage. *LLC* resonant converter is widely used as the dc–dc stage, because it achieves high efficiency as well as low EMI performance as a result of the inherent zero voltage switching (ZVS) on the primary metal oxide semiconductor field effect transistors (MOSFETs) and zero current switching (ZCS) on the secondary rectifiers [3]–[7].

A critical issue for server and data center power supply is the hold-up problem illustrated in Fig. 2. When the ac line fails, the 400-V bus voltage reduces continuously. It is desired the 12-V dc be maintained for several tens of milliseconds, until the uninterruptible power system takes over [7]. If the operation range of the dc–dc converter is extended, the capacitor value used on the 400-V bus can be reduced, then the cost will drop and size will shrink significantly. Therefore, improving the operational input voltage range, i.e., the voltage gain of the dc–dc converter, is the solution to the hold-up issue.

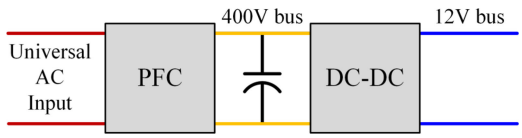

Fig. 1. Structure of the front-end converter in server and data center power supply.

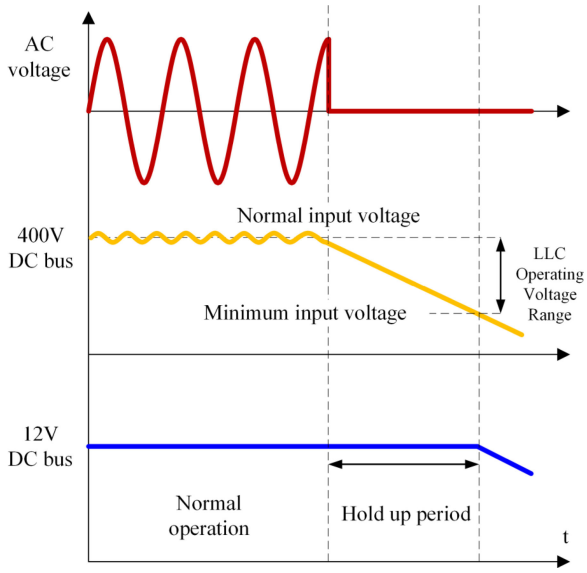

Fig. 2. Bus voltage behaviors during ac failure (hold-up process).

Conventional *LLC* is not suitable for hold-up operation. If an *LLC* converter is designed to operate over a wide input voltage range, the efficiency at nominal 400-V input will be severely compromised [8], [9]. Therefore, to solve the hold-up problem, *LLC* converter should be improved to meet the following requirements:

1) to optimize the nominal 400-V input operation to achieve high efficiency;

Manuscript received April 14, 2016; revised July 13, 2016; accepted August 15, 2016. Date of publication August 31, 2016; date of current version February 11, 2017. Recommended for publication by Associate Editor Y. Xing.

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Digital Object Identifier 10.1109/TPEL.2016.2604368

2) to increase the operational input voltage range of the *LLC* converter.

To achieve high efficiency at 400-V operation, the transformer turns ratio needs to be properly designed to ensure that the converter operates at resonant frequency at 400-V input. Moreover, the magnetizing inductance value should be optimized to reduce the circulating current in the resonant tank as much as possible, while maintaining ZVS for the half-bridge (HB) MOSFETs. At last, for 12-V output applications, on the secondary side, synchronous rectifiers (SR) should be used instead of diode rectifiers, as the forward voltage drop of diodes would be a deal breaker of the whole efficiency [9]–[12].

To improve the *LLC* converter's operational voltage range to meet hold-up time requirement, quite a few methods have been proposed. Among them, the most straightforward way is to employ a cascaded structure with a baby boost converter [13]. However, the additional power stage will reduce the efficiency at nominal 400-V operation. Besides, the two-stage configuration is complicated, and, consequently, costly.

To avoid degrading the 400-V efficiency, it is more reasonable to use a parallel-functioning structure rather than the aforementioned cascaded structure. The design of the *LLC* converter parameter should be emphasized on achieving high efficiency for normal operation and ignore the limited input voltage range. It is desired that an auxiliary voltage-gain improving circuit is added to the 400-V-optimized *LLC* converter. When the input voltage is at around normal level, the auxiliary circuit remains idle, and the *LLC* converter operation is not influenced. When the input voltage is lower than the designed input voltage range, the auxiliary circuit takes effect to improve the voltage gain and maintains the output voltage at desired level. Based on this idea, more effective methods have been developed, and will be described and analyzed in the following.

A method to solve the hold-up problem is to use auxiliary windings on the secondary side of the main transformer [14], [15]. When the input voltage is lower than the designed input voltage range, the switch-controlled auxiliary windings will take over the secondary-side power transfer. Increased transformer turns ratio helps us to achieve higher output-to-input voltage gain of an *LLC* converter during the hold-up period. The discrete parameter designs between nominal 400-V operation and hold-up mode operation can maintain 400-V input operation uninfluenced. However, usually the main transformer is the most bulky and lossy part of a converter; thus, adding extra windings makes it even more difficult to optimize the transformer from both efficiency and power density improvement point of view.

By driving the HB MOSFETs with asymmetric pulse-width modulation (APWM) rather than conventional frequency modulation (FM), *LLC* converter can improve voltage gain without any additional components [16]. This method, however, suffers from limited peak gain enhancement. Besides, once the resonant tank is designed, the maximum gain that APWM control could achieve is also determined. Thus, in order to satisfy the voltage gain requirement, the resonant parameters design might not be optimized for 400-V operation.

A critical insight was revealed in [17] that if the resonant tank can be charged with more energy during one switching cycle, *LLC* converter achieves higher gain. To charge the resonant tank more, the secondary windings are short-circuit for a certain period of time in every switching cycle. The downside of this method is that quite a few components need to be added in the power train on the secondary side, which causes size increasing and efficiency reducing.

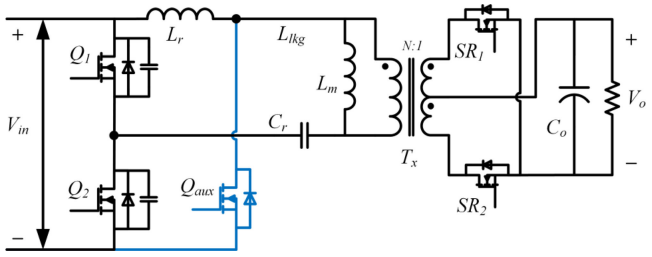

Fig. 3. Proposed sLLC converter with center-tapped transformer and SR.

Based on [17], a few improving methods have been proposed to adopt either boost PWM discontinuous-current mode control [18] or phase shift control on *LLC* topology [19], [20]. The common principle of these methods is that, in each switching cycle, the resonant tank will be short-circuited on either primary side or secondary side by auxiliary switches for a period of time so that the resonant inductor can be energized more quickly, hence store and transfer more power. The nominal 400-V efficiency remains uninfluenced as compared to a conventional *LLC* optimized for 400-V input voltage. For [18], the secondary rectifier current is more than four times higher in hold-up mode operation as the conduction time is very short. For [19] and [20], full-bridge rectifiers must be used for phase shift control. These traits make these methods less appealing in low-voltage and high-power applications.

In this paper, a family of *LLC* converters with auxiliary switch (sLLC) is proposed to solve the hold-up problem while avoiding the aforementioned issues. The proposed sLLC converters are able to operate with center-tapped transformer and SR; thus, it is particularly suitable for low-voltage high-current applications in data center and similar applications. The design for hold-up operation is independent of nominal 400-V operation design; thus, the converter achieves optimal efficiency at nominal 400-V input. During hold-up period, the auxiliary switch operates in the PWM mode. When the auxiliary switch is turned on, the resonant inductor absorbs power directly from the input dc bus, rather than from the resonant capacitor in the conventional *LLC* converter; thus, the resonant inductor accumulates more energy in shorter time and high-voltage gain is achieved.

This paper is organized as follows: Section II explains the operation principle; Section III and Section IV provide detailed circuit analysis; Section V shows additional sLLC topologies; Section VI demonstrates the experimental results; and Section VII concludes this paper.

II. Operation Principle and Mode Analysis of the Proposed Converter

A. Operation Principle of the Proposed sLLC Converter

Fig. 3 shows an example of the proposed HB *LLC* converter with auxiliary switch (sLLC) for hold-up operation. Only one MOSFET $Q_{\rm aux}$ is added to the conventional *LLC* converter.

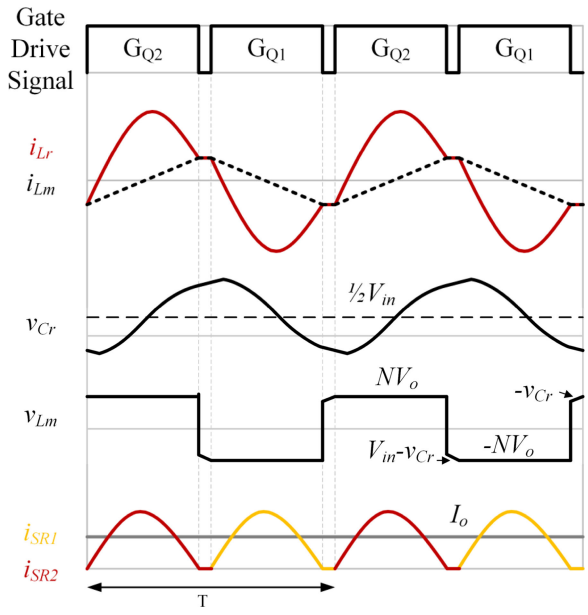

Fig. 4. Key waveforms of the sLLC converter for nominal 400-V operation.

The magnetizing inductor L_m can be integrated into the main transformer, while the resonant inductor L_r and resonant capacitor C_r are external. Besides, the added MOSFET is ground referenced so that the driver design is simple.

This topology will be used to explain the operating principle and demonstrate the experiment results. Other sLLC topologies in the family have the same operation principle and similar results and will be analyzed in a section later.

When the input voltage is around nominal 400 V, the auxiliary switch is kept off. The sLLC converter operates just like the conventional HB *LLC* converter. Thus, all the desirable features of *LLC* converters are automatically retained. Besides, the parameter design of the resonant components (L_r, C_r, L_m) only considers nominal 400-V efficiency. The magnetizing inductor could be of relatively large value to reduce the circulating magnetizing current and to improve the efficiency. FM is still used to regulate the output voltage when the input voltage reduces slightly (i.e., switching frequency reduces with input voltage reducing). This is good to address the low-frequency fluctuation on 400-V bus from the PFC stage. The key waveforms are shown in Fig. 4.

In Fig. 4, G_{Q1}, G_{Q2} are the gate signals of the HB switches; $i_{\rm Lr}$ and $i_{\rm Lm}$ are the resonant inductor current and the magnetizing current on the primary side; $v_{\rm Cr}$ is the voltage stress across resonant capacitor; $v_{\rm Lm}$ is the voltage on the magnetizing inductor; $V_{\rm in}$ and V_o are the input and output voltages; N is the transformer turns ratio; $i_{\rm SR1}$ and $i_{\rm SR2}$ are the secondary SR current; and I_o is the average load current. If the input voltage reduces to a level that the *LLC* converter cannot maintain the required output voltage level with FM, HB MOSFET will operate at the minimum switching frequency, and the auxiliary switch operates in the PWM mode. The key waveforms of the proposed sLLC converter during hold-up period is shown in Fig. 5, in which G_{Q1}, G_{Q2}, and $G_{\rm Qaux}$ are the gate signals; $i_{\rm Qaux}$ is the current stress in the auxiliary switch. During the positive half cycle when Q_2 is ON (input source injects energy to the

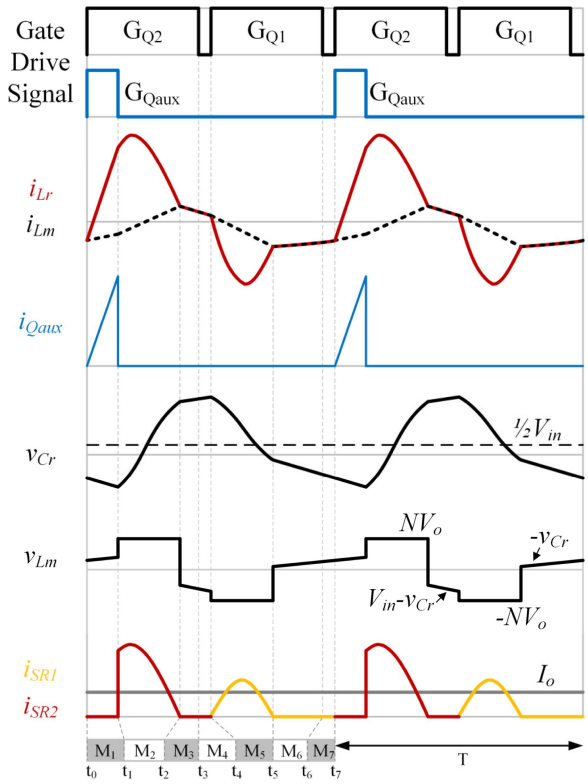

Fig. 5. Key waveforms of the sLLC during hold-up period.

resonant tank), the auxiliary switch $Q_{\rm aux}$ turns ON for certain period of time in one switching period, allowing the resonant inductor to be charged directly by the bus voltage. The longer the auxiliary switch conducts, the more energy will be stored and transferred, the higher gain can be achieved.

The proposed method improves the voltage gain from increase the energy stored in the resonant inductor point of view. In the conventional *LLC* converter, all input power will go through the capacitor. Thus, the capacitor could be view as a varying voltage source from which the inductor absorbs energy solely. While in the proposed sLLC converter, the inductor also absorbs energy from the input bus when the auxiliary switch is turned on. This part of energy is drained to the load directly, and does not appear on the resonant capacitor. Thus, the resonant inductor absorbs energy from both the capacitor and the input bus. Consequently, more energy could be stored in the inductor and higher voltage gain could be achieved.

B. Mode Analysis of the Proposed sLLC Converter

The *LLC* operation equivalent circuits of different mode have been extensively studied in many literatures, thus will not be covered in this paper. The sLLC operation of different modes during hold-up period will be explained. During hold-up period, the operation in each switching cycle can be divided into seven modes (M1–M7). The equivalent circuits are shown in Fig. 6.

Mode 1 (M1): Q_2 and $Q_{\rm aux}$ are turned ON at t_0. L_r will be charged by the bus voltage so that $i_{\rm Lr}$ increases linearly and sharply. L_m and C_r will short-circuited and resonate. The magnetizing current is negative during M1. No current will go through the transformer, and the output capacitor C_o discharges.

Fig. 6. Equivalent circuit of the proposed sLLC converter in hold-up operation. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7.

Mode 2 (M2): $Q_{\rm aux}$ turns OFF at t_1, while Q_2 remains ON. L_r current will be released through the transformer. $\rm SR_2$ will conduct to charge C_o. The transformer will be clamped by the output voltage V_o, thus magnetizing inductor current $i_{\rm Lm}$ increase linearly. At t_2, $i_{\rm Lr}$ meets $i_{\rm Lm}$, and the SR current reduces to zero.

Mode 3 (M3): In M3, L_m will resonate together with L_r and C_r. Transformer is in idle mode while the load current is provided by C_o. At t_3, Q_2 is turned OFF.

Mode 4 (M4): Both Q_1 and Q_2 are OFF during M4, the dead time. The resonant current will charge the parasitic capacitor of Q_2 while discharge that of Q_1. When the voltage across Q_1 drops to zero or so, the body diode of Q_1 conducts, clamping the voltage of Q_1 at around 0 V, thus ZVS is achieved for Q_1 when it is turned on at t_4.

Mode 5 (M5): L_r and C_r will resonate in M5 with Q_1 ON. $\rm SR_1$ conducts to charge C_o and powering the load. The transformer will be reversely clamped by the output voltage V_o, thus magnetizing inductor current $i_{\rm Lm}$ decrease linearly. At t_5, $i_{\rm Lr}$ meets $i_{\rm Lm}$, and $i_{\rm SR1}$ drops to zero.

Mode 6 (M6): L_m will resonate jointly with L_r and C_r in M6. Transformer power transfer is cutoff while the load current is provided by C_o. At t_6, Q_1 is turned OFF.

Mode 7 (M7): M7 is the dead time that the HB switches are off. The parasitic capacitor of Q_1 will be charged and that of Q_2 discharged by the resonant current. ZVS is achieved for Q_2 when it is turned on at t_7.

After M7, Q_2 and $Q_{\rm aux}$ will be turned ON, and the converter operates in M1 again.

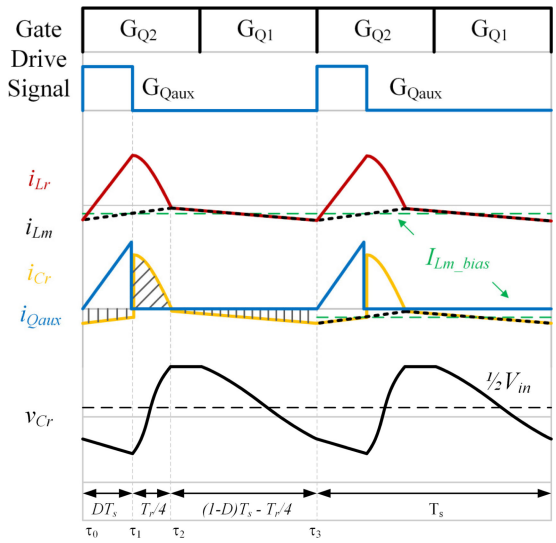

Fig. 7. Key waveforms of the simplified sLLC converter in extreme case.

In this section, an example of the proposed sLLC converter family is introduced. The voltage gain improving principle and detailed operation modes during hold-up time are explained.

III. Simplified Operation Modes and Assumptions for Circuit Analysis

When the input voltage is around 400 V, the operation of the proposed sLLC converter is exactly the same as that of the conventional *LLC* converter. The analysis of conventional *LLC* converter with FM will not be covered in this paper, as many publications already have extensive studies of conventional *LLC* in terms of peak gain, components stresses, dead time optimization, etc. [21]–[33]. *LLC* converter naturally has no closed-form solution of currents and voltages due to the nonlinear characteristics [32]–[35], which add a lot of difficulties for the designer. To relieve the complexity of the design process, the equivalent circuit of the sLLC converter in each mode is simplified to obtain closed-form solution in this section. The mathematic analyses in the next section are made based on the assumptions below.

A. Assumption of Extreme Case Behavior

As stated in Section II, the resonant tank absorbs power only in the positive half cycle. It can be inferred that, for given load power, when the duty cycle of the auxiliary switch increases, the resonant inductor current $i_{\rm Lr}$ increases in the positive half cycle, while decreases in the negative half cycle. It is observed that when the duty cycle is beyond certain value, the power transfer in the negative half cycle will reduce to zero, and the resonant inductor current $i_{\rm Lr}$ will always be equal to the magnetizing current $i_{\rm Lm}$ during the negative half cycle. The analysis in this section will be based on the assumption that all load power is transferred during the positive half cycle, as it indicates the extreme operation condition in terms of the voltage gain capacity, as well as the worst case in terms of component stresses.

Fig. 7 shows the waveforms of the simplified sLLC converter in extreme case. In addition to the nomenclature used in Fig. 5, $i_{\rm Cr}$ is the current in the resonant capacitor; $I_{\rm Lm\_bias}$ is the dc bias in the magnetizing inductor; D is the duty cycle of the auxiliary switch; T_s is the cycle period in correspondence to the minimum switching frequency f_s that $T_s = 1/f_s$; andT_r is the period of a resonant cycle that $T_r = 2\pi\sqrt{L_r C_r}$. To distinguish the simplified model from the previous model, the time instant will be defined as $\tau_0, \tau_1 \ldots$ instead of $t_0, t_1 \ldots$ used in Fig. 5.

In this paper, the analysis is conducted specifically at the peak gain frequency of the resonant tank to make full use of the FM. If the designer wish to use narrower input voltage range or narrower frequency range, the proposed analytical method could still be applied. However, then PWM near the resonant frequency is not preferred, because operating the HB switches and the auxiliary switch at lower frequency will help the converter achieve higher voltage gain than near the resonant frequency.

B. Approximation of Timing

The *LLC* topology has no closed-form solution as it involves trigonometric equation sets and requires iteration process with proper initials. To reach a design decision based on strict circuit analysis will greatly increase the time cost. Thus, in this paper, analytical expressions with no closed-form solutions are avoided consciously. To simplify the circuit behaviors, while maintaining reasonable accuracy, it is noticed that timing in the operation of auxiliary switch is trackable clue. Fixed resonant period will be used to breaks the closed equation sets, and enables simple closed-form expressions by piecewise functions with known timing.

In one switching cycle, timing can be based on the resonant inductor current. During τ_0 to τ_1, the time interval DT_s, the auxiliary switch $Q_{\rm aux}$ is ON. The resonant inductor current $i_{\rm Lr}$ increases linearly. The magnetizing current $i_{\rm Lm}$ also increases as the negative capacitor voltage will be reversely across the transformer. Instantaneously $Q_{\rm aux}$ turns OFF, $i_{\rm Lr}$ resonates in a sinusoidal shape until it meets $i_{\rm Lm}$. This period of time (τ_1 to τ_2) is roughly $T_r/4$. It could be understood in the means that $i_{\rm Lr}$ reduces from the peak value to 0 in a quarter of one resonant cycle period of L_r and C_r. To maintain ZCS on the secondary rectifiers, τ_2 should occur before Q_2 is OFF, and this limits the maximum value for duty cycle D at around 0.25. The actual time length from τ_1 to τ_2 may vary according to the duty cycle D. Generally speaking, when the duty cycle is relatively large, e.g., $D = 0.2$, the resonant period is slightly below $T_r/4$ and vice versa. To simplify the calculation, it is assumed that the resonant period is fixed at $T_r/4$. In the rest of the switching cycle from τ_2 to τ_3, no power will be transferred to the load and $i_{\rm Lr}$ equals to $i_{\rm Lm}$.

Theoretically, the maximum duty cycle is set at 0.25 based on the ZCS operation of the rectifiers. In practice, the maximum duty cycle could be limited by the voltage stress of the auxiliary switch as the leakage inductor from the transformer is inevitable. Using low-voltage rating MOSFET as the auxiliary switch could reduce the circuit cost, while high-voltage rating switch could increase the duty cycle, and, thus, the voltage gain. In nutshell, the designer should tradeoff between the performance and cost in a specific design.

TABLE I
SPECIFICATIONS OF THE sLLC CONVERTER

Input voltage	250–400 V
LLC FM range	320–400 V
sLLC PWM range	250–320 V
Minimum switching frequency	150 kHz
Output voltage/power	12 V/ 300 W
Transformer turns ratio	17:1
Resonant inductor	24 μH
Resonant capacitor	12 nF
Magnetizing inductor	250 μH
Leakage inductor	6 μH
Output capacitor	2 mF
HB MOSFETs	IPW60R190C6
SR MOSFETs	SiRA00DP
SR driver	IR11682s
Auxiliary capacitor	2 nF
Auxiliary MOSFET	IPB65R110CFD
Auxiliary diode	APT60D60BG

C. Approximation of Resonant Tank Currents

In real case, the magnetizing current $i_{\rm Lm}$ is linear only when the power stage transfers power to the load; otherwise, $i_{\rm Lm}$ should be in sinusoidal shape whose frequency is $f_m = 1/2\pi\sqrt{(L_r + L_m)C_r}$. In this approximation, the magnetizing current $i_{\rm Lm}$ will have a triangular shape. More details will be included in the following part.

When the duty cycle of the auxiliary switch *D* is high, resonant current $i_{\rm Lr}$ is of much higher value than the magnetizing current $i_{\rm Lm}$ so that $i_{\rm Lm}$ can be neglected in $i_{\rm Lr}$ dominated calculation. Currents in the parasitic components will also be neglected.

D. Assumption of Resonant Tank Parameters

As the parameter design for hold-up mode is independent from 400-V case, it is assumed that a set of well-designed resonant tank parameters are already obtained to achieve high efficiency for 400-V operation. Thus, it could also be assumed that some key circuit information is obtained from either calculation or simulation, including the minimum switching frequency f_s, the peak voltage gain at f_s, and the current stresses in the resonant tank, etc. Parameters and specifications in Table I will be used as an example for the analysis. With different parameter designs, the topology will work with the same principle and the analytical method can still be applied.

IV. CIRCUIT ANALYSIS OF THE PROPOSED CONVERTER

In this section, key circuit characteristics and design considerations of the proposed sLLC converter during hold-up period will be discussed. Behaviors of the equivalent circuit in each mode will be analyzed and expressed in fundamental physics and mathematics. The closed-form solutions for component stresses could be used to reach a quick and accurate decision during the designing process.

A. Current Stress of Auxiliary Switches $Q_{\rm aux}$

The auxiliary switch $Q_{\rm aux}$ will always operate at minimum switching frequency, thus the cycle period is fixed at T_s. Supposed the time length between τ_0 to τ_1 is $T_{\rm on\_aux}$, during which $Q_{\rm aux}$ is ON, then the duty cycle *D* can be defined as

$$D = \frac{T_{\rm on\_aux}}{T_s}. \tag{1}$$

When the auxiliary switch $Q_{\rm aux}$ turns ON at τ_0, the current $i_{\rm Qaux}$ increases from zero linearly. At τ_1, $Q_{\rm aux}$ turns OFF and $i_{\rm Qaux}$ reaches the peak value $I_{\rm Qaux\_pk}$, which can be expressed by

$$I_{\rm Qaux\_pk} = \frac{V_{\rm in}}{L_r} \cdot DT_s. \tag{2}$$

The RMS current in $Q_{\rm aux}$ can be obtained as

$$I_{\rm Qaux\_rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} I_{\rm Qaux}^2(t)dt} = \frac{V_{\rm in}}{L_r} \cdot DT_s \cdot \sqrt{\frac{D}{3}}. \tag{3}$$

Most of time, $Q_{\rm aux}$ will not be operating. Even during the hold-up period, it operates only for several tens of milliseconds. Thus, peak current rating rather than RMS current rating should be primarily considered when selecting parts for $Q_{\rm aux}$. Generally speaking, more aggressive strategy could be taken from the stand of cost.

B. Current Stress for HB MOSFET

As stated in *Assumption* in Section III-A, the current stress in the top HB switch $i_{\rm Q1}$ reduces with the duty cycle *D* increasing. When *D* increases to a level that no power is transferred during the negative half cycle, i_{Q1} will be equal to the magnetizing inductor current $i_{\rm Lm}$, which is relatively low.

For the bottom HB switch, the current stress increases with *D* increasing. Take the numbers in Table I, comparing to the worst case in the *LLC* normal operation, the input voltage reduces from 320 to 250 V during hold-up period. This means the input current has to increase 1.28 (320/ 250) times in the primary side. When the negative half cycle does not provide power to the load, the current stress in the bottom switch will be doubled, which make the total stress 2.56 ($1.28 * 2$) times the worst case in normal operation. Considering the presence of the negative dc bias current, which also go through the HB switches, the peak current stress in the bottom switch could be 1.5–2.5 times of that in normal operation. So is the RMS current. However, the hold-up period usually lasts for several tens of milliseconds only. For the most part, the MOSFETs can survive for that short period of time before reaching the thermal constraint.

The conclusion for the HB MOSFETs selection would be that normal operation for 400-V condition should be the primary consideration.

C. Current Stress and Driving Scheme for SR MOSFET

SR current stress is determined by the primary-side resonant current. The peak current stress in SR will reach its maximum when the duty cycle of auxiliary switch reaches the suggested upper limit. Neglecting the magnetizing current, the peak current stress could be calculated by (4), where *N* is the transformer turns ratio

$$I_{\rm SR\_pk} = {\rm NI}_{\rm Qaux\_pk} = N\frac{V_{\rm in}}{L_r} \cdot DT_s. \tag{4}$$

During τ_1 to τ_2, the inductor L_r will resonate with the resonant capacitor $C_{\rm r}$, and the current will be transferred to the output side through SR. As explained in Chapter III, the time for the resonance is close to $T_r/4$. Based on the above information, the RMS current stress in SR could be calculated by

$$I_{\rm SR\_rms} = \sqrt{\frac{1}{T_s}\int_{\frac{T_r}{4}}^{\frac{T_r}{2}}\left[I_{\rm SR\_pk}\cdot\sin\left(\frac{2\pi}{T_r}t\right)\right]^2 dt} = N\frac{V_{\rm in}}{L_r}\cdot D\cdot\sqrt{\frac{1}{8f_r f_s}}. \quad (5)$$

The SR driving scheme for hold-up operation has the same principle as that for normal operation. The source p-i-n of the SR MOSFET is connected to the common ground of the secondary side. The voltage on the drain pin is fed to the controller as the trigger signal. When the voltage across the SR MOSFET drop to around -0.5 V, it is believed that the body diode is conducting, and the controller will turn on the SR MOSFET. During SR is on, voltage across the drain and source will be negative. When the SR voltage drops to zero or so, it is believed that the current has reduced to zero, and the controller will turn the SR MOSFET off. In order to compensate the impact of the package inductor, a RCD delay circuit [12] has been used to help the controller to capture the proper timing.

During the hold-up period, as the switching frequency is below the resonant frequency, ZCS operation can be achieved; thus, the turn off timing can still be compensated by the same RCD delay circuit for normal operation. When the auxiliary switch turns off, the resonant current will be transferred to the load through SR. Though the current might increase with a steep slope, it still starts from zero. Thus, the turn on instant is also same as normal operation.

If the design of the inductor ratio is very small, the SR could conduct during the auxiliary switch on-state. However, this is not a common case in the sLLC converter, as the 400-V design usually requires the inductor ratio to be high. Besides, even if it happens, the overall circuit behavior does not change much, and the bottom switch ZVS operation will not be sacrificed.

D. Output-to-Input DC Voltage Gain (Conversion Ratio)

For both conventional HB *LLC* converter and the proposed sLLC converter, energy exchange between source and the resonant tank occurs only in the positive half cycle [35], [36].

For the conventional HB *LLC* converter, in each switching cycle, during Q_2 is ON, the time integral of the input current $i_{\rm input}$ (equals to i_{Q2} and $i_{\rm Lr}$) is the total input charge. The total input energy in one switching cycle can then be calculated by multiplying the input charge by the input bus voltage. The output energy in one switching cycle is determined by the average output power and the switching frequency. Assuming 100% efficiency and steady-state operation, the input energy is equal to the output energy according to energy conservation law. Considering constant load current, the relation can be expressed as

$$V_{\rm in}\cdot\int_0^{\frac{T_s}{2}} i_{\rm input}(t)dt = \frac{V_o\cdot I_o}{f_s}. \quad (6)$$

For the proposed sLLC converter, the total input current is comprised of two parts $-i_{Q2}$ and $i_{\rm Qaux}$, which is illustrated in Fig. 7. i_{Q2} represents the energy absorbed by the whole resonant tank, while $i_{\rm Qaux}$ stands for the energy accumulated on the resonant inductor alone—no exchange with the capacitor. It is observed that the total net charge through Q_2 remains the same in spite of the duty cycle D of the $Q_{\rm aux}$ provided the converter is operating with the same input voltage and switching frequency in steady state. This automatically implies that the total charge through $Q_{\rm aux}$ contributes to the voltage gain improvement solely.

According to the *Assumption* in Section III-D, the parameters of the resonant tank are well designed, the circuit parameters have been obtained through simulation or calculation for *LLC* operating at normal input voltage.

Denote $V_{o,0}$ as the output voltage for input voltage $V_{\rm in}$ with duty cycle $D=0$ at minimum switching frequency f_s. It should be noted that $2N\cdot V_{o,0}/V_{\rm in}$ corresponds to the *LLC* peak voltage gain $G_{\rm pk}$ that can be achieved by FM. According to (6), the energy conservation relation can be expressed in (7), in which $Q_{\rm Q2,0}$ is the charge through Q_2 when $D=0$

$$V_{\rm in}\cdot Q_{Q2,0} = \frac{V_{o,0}\cdot I_o}{f_s}. \quad (7)$$

Denote $V_{o,D}$ as the output voltage for input voltage $V_{\rm in}$ and duty cycle D. According to (6), the energy conservation relation can be expressed in (8), in which $Q_{Q2,D}$ is the total charge through Q_2; and $Q_{{\rm Qaux},D}$ is the total charge through $Q_{\rm aux}$, which is given in (9):

$$V_{\rm in}\cdot Q_{Q2,D} + V_{\rm in}\cdot Q_{{\rm Qaux},D} = \frac{V_{o,D}\cdot I_o}{f_s} \quad (8)$$

$$Q_{{\rm Qaux},D} = \frac{1}{T_s}\int_0^{T_s} I_{\rm Qaux}(t)dt = \frac{V_{\rm in}}{2L_r}\cdot D^2 T_s^2. \quad (9)$$

Define the voltage gain achieved by the PWM control as $G_{\rm PWM} = 2N\cdot V_{o,D}/V_{\rm in}$. Connecting (7)–(9) and considering $Q_{Q2,0} = Q_{Q2,D}$, then $G_{\rm PWM}$ could be calculated as

$$G_{\rm PWM} = \frac{2N\cdot V_{o,0}}{V_{\rm in}} + \frac{N\cdot V_{\rm in}\cdot D^2}{L_r\cdot I_o\cdot f_s}. \quad (10)$$

Equation (10) represents the voltage gain improving trend and capacity of the proposed sLLC converter. The expression of $G_{\rm PWM}$ contains two parts: the first part is the peak voltage gain achieved by FM; the second part reflects the voltage gain achieved by the PWM controlled auxiliary switch. When $D=0$, the minimum voltage gain achieved by PWM is equal to the maximum voltage gain achieved by FM, which results in a seamless output voltage regulation.

Equation (10) contains only one variable, the duty cycle D. Other parameters can be either obtained directly or calculated from the specification of the design. For example, if L_r, C_r, L_m are determined as those in Table I, then through PSIM simulation, the minimum switching frequency is 150 kHz, at which the peak voltage gain $G_{\rm pk}$ is around 1.3 for 25-A load. If the input voltage reduces to 250-V, *LLC* output voltage $V_{o,0}$ at 150 kHz is 9.5 V. For 250-V input, the required voltage gain

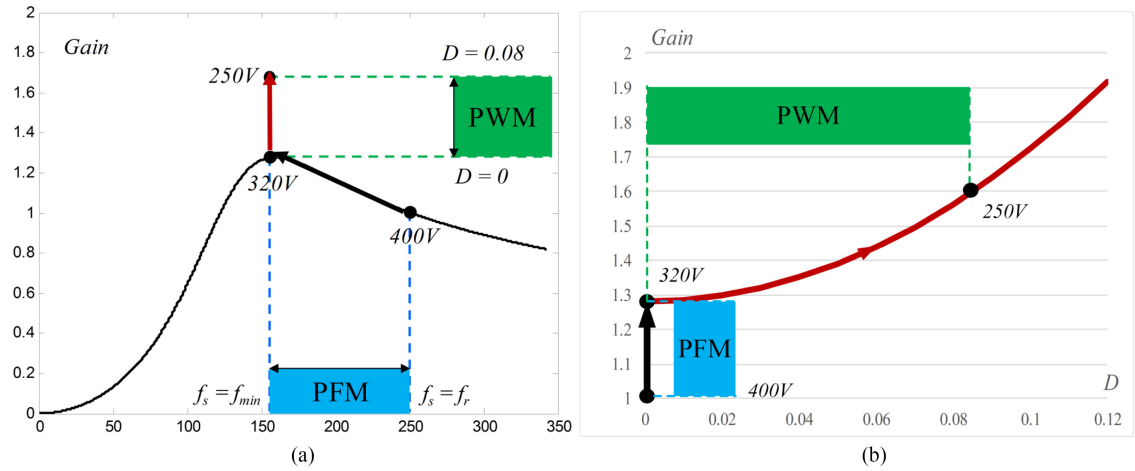

Fig. 8. G_{PWM} versus f_s and G_{PWM} versus D.

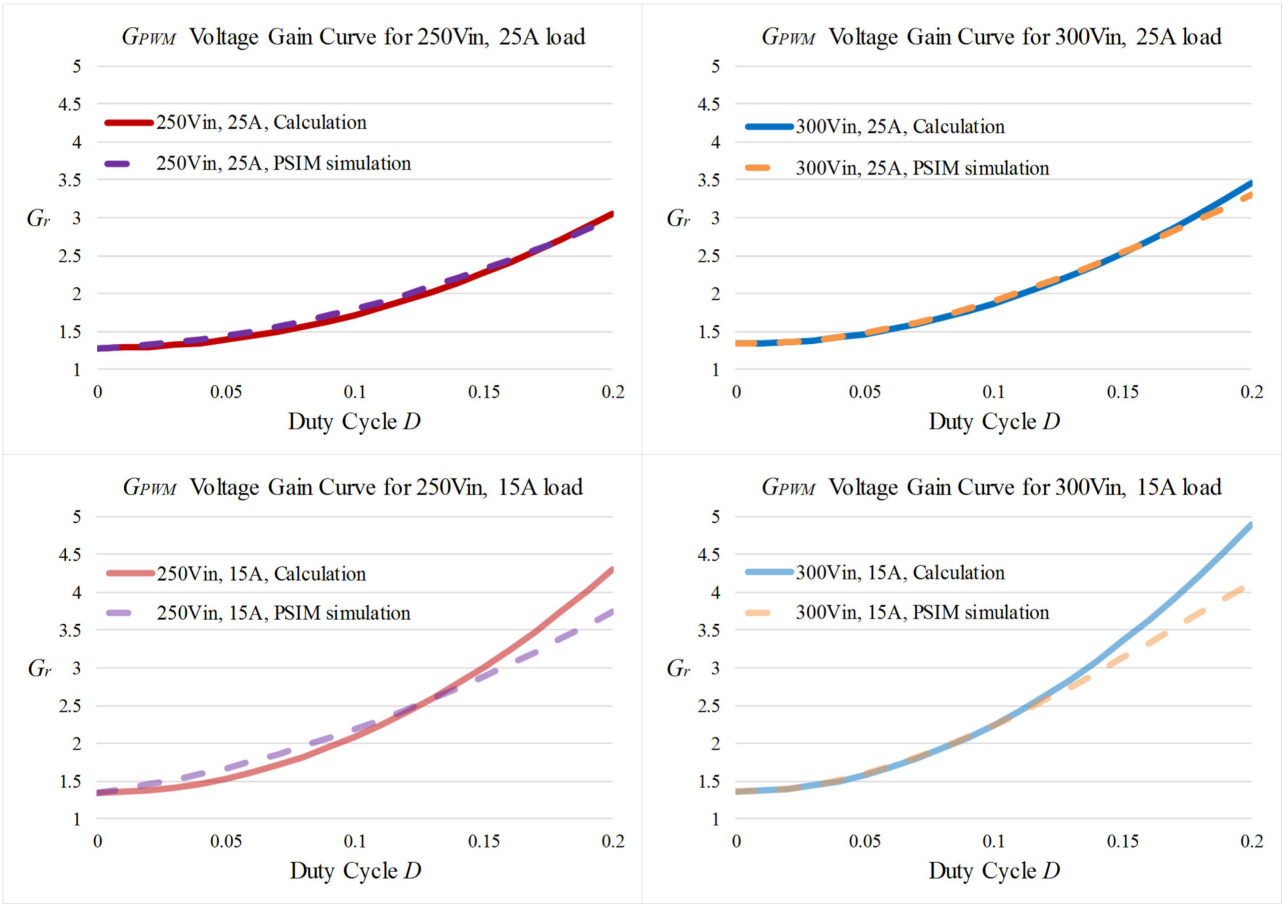

Fig. 9. Voltage gain of PWM of the sLLC converter for different cases.

is $G_{\mathrm{required}} = 400/250\ \mathrm{V} = 1.6$. Then, from (10), the required duty cycle of Q_{aux} can be calculated as 0.08.

The comparison of PFM and PWM control is shown in Fig. 8. Black line shows the voltage gain curve by PFM, and the red line shows the voltage gain improvement by PWM control.

Fig. 9 shows the voltage gain curve with PWM under 250-V input 25-A load case, 300-V input 25-A load case, 250- V input 15-A load case, and 300-V input 15-A load case, respectively. Calculation from (10) and PSIM simulation results are compared. It should be noted that in real situation, D value is usually small and $D = 0.2$ is relatively large duty cycle. As can be observed, even under the worst case—250-V input 25-A load—the voltage gain can reach 3 as compared to 1.3 at $D = 0$.

The voltage gain of the *LLC* converter increases greatly with load power reducing. It could be proved with PSIM simulation that at 10-A load, the *LLC* converter could operate at 250-V

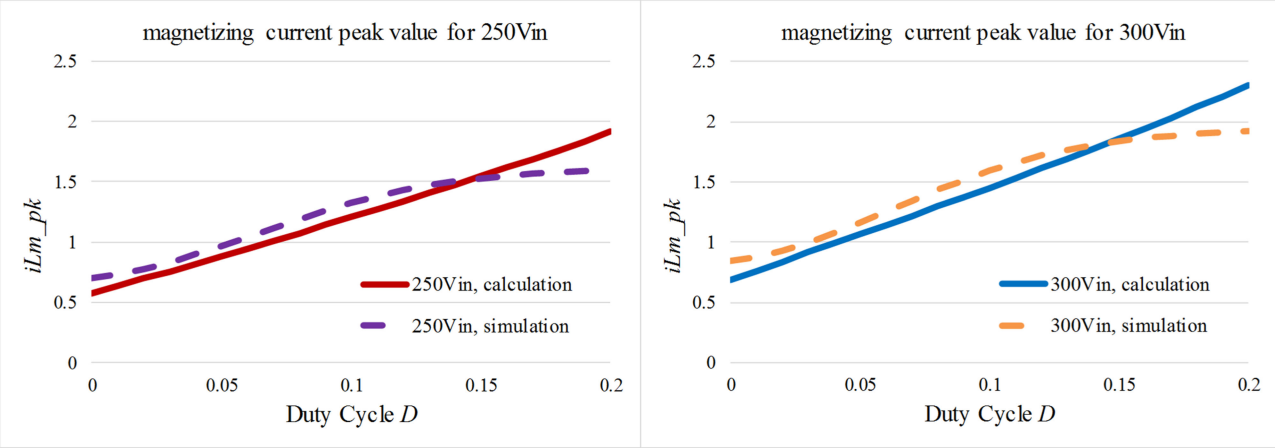

Fig. 10. Magnetizing current peak value for 250- and 300-V input.

input with FM alone, and the auxiliary switch does not need to operate.

E. Magnetizing Current With DC Bias

The asymmetrical current waveform between positive half cycle and negative half cycle will introduce a dc bias $I_{\mathrm{Lm\_bias}}$ on the magnetizing inductor current. In steady state, ampere–second balance must be achieved on the resonant capacitor. Neglecting the magnetizing current from τ_1 to τ_2, then $I_{\mathrm{Cr\_pk}}$ is equal to $I_{\mathrm{Qaux\_pk}}$, and $I_{\mathrm{Lm\_bias}}$ can be obtained as

$$I_{\mathrm{Lm\_bias}} = -\frac{1}{T_s}\int_{\frac{T_r}{4}}^{\frac{T_r}{2}} I_{\mathrm{Cr\_pk}} \sin\left(\frac{2\pi}{T_r}t\right)dt = -V_{\mathrm{in}} D\sqrt{\frac{C_r}{L_r}}. \tag{11}$$

The magnetizing current reaches the maximum value $I_{\mathrm{Lm\_max}}$ at time instant τ_2, and the minimum value $I_{\mathrm{Lm\_min}}$ occurs near the time instant τ_0. The magnetizing inductor current is sinusoidal and near symmetrical during time interval τ_0 to τ_1 and τ_2 to τ_3. Thus, it is reasonable to assume that the slope of the linearized magnetizing current is of the same absolute value. Assuming the slope is k, the peak-to-peak value of I_{Lm} can be found in (12), in which $V_o = G_{\mathrm{PWM}} \cdot V_{\mathrm{in}}/2N$

$$\Delta I_{\mathrm{Lm}} = kDT_s + \frac{nV_o}{L_m}\frac{T_r}{4} = k\left[(1-D)\,T_s - \frac{T_r}{4}\right]. \tag{12}$$

Then, the peak value of the magnetizing current can be obtained by (13), which can be used to calculate the transformer core size, dead time of the HB switches, etc

$$\begin{aligned} I_{\mathrm{Lm\_pk}} &= -I_{\mathrm{Lm\_min}} = -\left(I_{\mathrm{Lm\_bias}} - \frac{\Delta I_{\mathrm{Lm}}}{2}\right) \\ &= V_{\mathrm{in}} D\sqrt{\frac{C_r}{L_r}} + \frac{nV_o}{L_m}\left(\frac{\pi\sqrt{L_r C_r}\,D}{2\,(1-2D) - \pi\sqrt{L_r C_r}\,f_s}\right. \\ &\quad \left. - \frac{\pi\sqrt{L_r C_r}}{2}\right). \end{aligned} \tag{13}$$

Fig. 10 shows the peak magnetizing current stress comparison between calculation and PSIM simulation. The magnetizing current is irrelevant of the load power, thus results of two different input voltages (250 and 300 V_{in}) are provided. From (13), it is noted that the peak magnetizing current stress is linearly related to the duty cycle D. The solid line shows calculated peak magnetizing current stress, and the dash line shows the results from PSIM simulation. As can be observed, the two results match well.

Compared to normal operation, it is certain that the dc bias will increase the maximum magnetizing current stress and total flux in the core. However, the dc bias will not cause saturation of the core, because it is common practice to add an air gap on the transformer core in order to integrate the magnetizing inductor. Besides, the hold-up period only takes for 20–50 ms. Thus, from the thermal point of view, the dc bias would not threaten the design of the original *LLC* converter.

F. Resonant Capacitor Voltage Stress

When the auxiliary switch operates, the energy stored in the resonant inductor is increased; however, this part of energy does not exchange with the capacitor and will be directly drained to the load side. Thus, the capacitor voltage stress remains the same despite the duty cycle of the auxiliary switch. For simplicity, the voltage stress on the capacitor will be calculated at $D = 0$.

At the transition boundary of PFM and PWM, the voltage gain reaches the peak of FM, where the resonant tank is at the boundary of inductive zone and capacitor zone—resistive. The resonant current (also input current) will be in phase with the input square-wave voltage. When the current crosses zero, the resonant capacitor voltage is at the minimum, as positive current will start to charge the capacitor afterwards. During the positive half cycle, the input charge will accumulate on the resonant capacitor whose voltage will reach the maximum when the positive half cycle ends. This could be described with

$$\Delta V_{\mathrm{Cr}} = V_{\mathrm{Cr\_max}} - V_{\mathrm{Cr\_min}} = \frac{1}{C_r}\int_0^{\frac{T_s}{2}} i_{\mathrm{input}}\,(t)dt. \tag{14}$$

Combining (14) with (8) and considering the $V_{\mathrm{in}}/2$ bias on C_r, the peak voltage stress on the resonant capacitor is given in

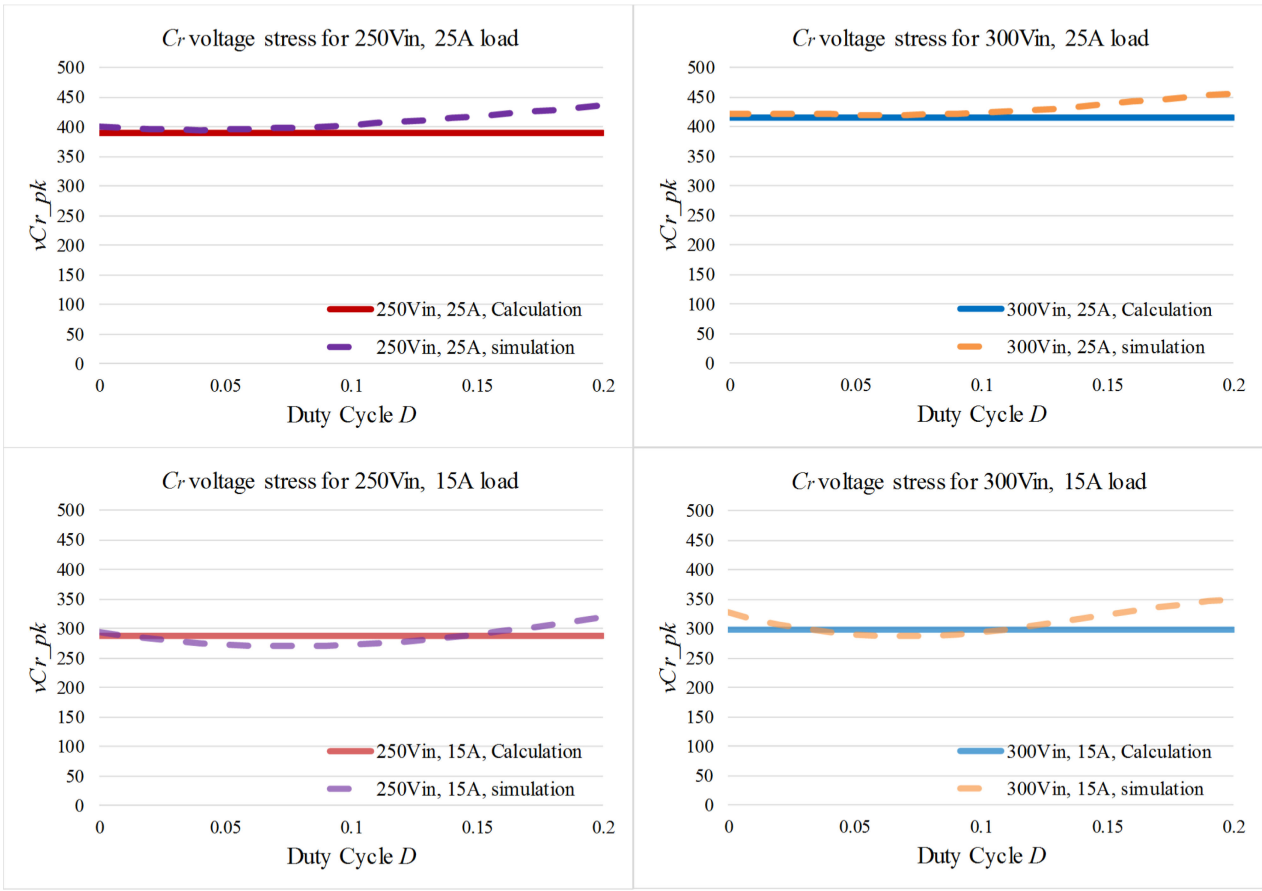

Fig. 11. Resonant capacitor peak voltage stress for 250 $V_{\rm in}$, 300 $V_{\rm in}$ and 15-, 25-A load conditions.

(15), which is essential for the resonant capacitor selection

$$V_{\rm Cr\_pk} = V_{\rm Cr\_max} = \frac{V_{\rm in} + \Delta V_{\rm Cr}}{2} = \frac{1}{2}\left(V_{\rm in} + \frac{V_{o,0} I_o}{V_{\rm in} C_r f_s}\right). \tag{15}$$

The simulation validation of the peak voltage stress on resonant capacitor is provided in Fig. 11. Results are provided for two input voltage levels (of 250 and 300 V) and two load current conditions (of 15 and 25 A). Equation (15) indicates that the peak voltage stress on C_r is irrelevant with duty cycle D, and, thus, the calculation result is a constant line in Fig. 11. The dash line shows the results from PSIM simulation. As can be observed, the calculation matches well with the simulation results.

In this section, key circuit characteristic is analyzed and expressed in closed-form equations to help the design of the sLLC converter, such as parameter and components selection.

V. sLLC Converter Family

Fig. 12 shows the complete HB sLLC converter family for hold-up operation. In Fig. 12 (a), the sLLC topology #1 has been selected as an example and analyzed in details in the previous sections. Compared with the other topologies in the family, sLLC #1 needs the least component count. Besides, the added MOSFET is ground referenced, thus the driver design is simple.

In sLLC topology #2, only one MOSFET $Q_{\rm aux}$ is added. In sLLC topology #3 to sLLC topology #6, a branch of series connected MOSFET $Q_{\rm aux}$ and diode $D_{\rm aux}$ is added, in which $D_{\rm aux}$ is used to provide unidirectional charging path from 400-V bus to the primary ground. In all six topologies, the magnetizing inductor L_m can be integrated into the main transformer, while the resonant inductor L_r and resonant capacitor C_r are external.

Compared to sLLC topologies #1, same operation and similar results can be achieved by other topologies in the family. Take topology #6 as an example, during hold-up operation, when Q_1 turns ON, $Q_{\rm aux}$ will also turn ON for a period of time, thus L_r accumulates energy quickly with the input voltage, while no power is transferred to the load. As $Q_{\rm aux}$ turns OFF, Q_1 will still be conducting, and then the energy stored in L_r will be transferred to the load. When Q_2 turns ON, $Q_{\rm aux}$ will remain OFF, thus the operation is the same as conventional *LLC* converter. Depending on the conducting time of $Q_{\rm aux}$, the voltage gain of the converter can be increased.

Fig. 13–15 show the PSIM simulation results of topology #6. Specifications in Table I are used for the simulation.

In Fig. 13, the input voltage is 400 V, at which the converter operates for dominantly long time. The switching frequency is 260 kHz, which is near the resonant switching frequency. Magnetizing inductor current is designed to be low, thus the circulation energy is low, and high efficiency can be achieved.

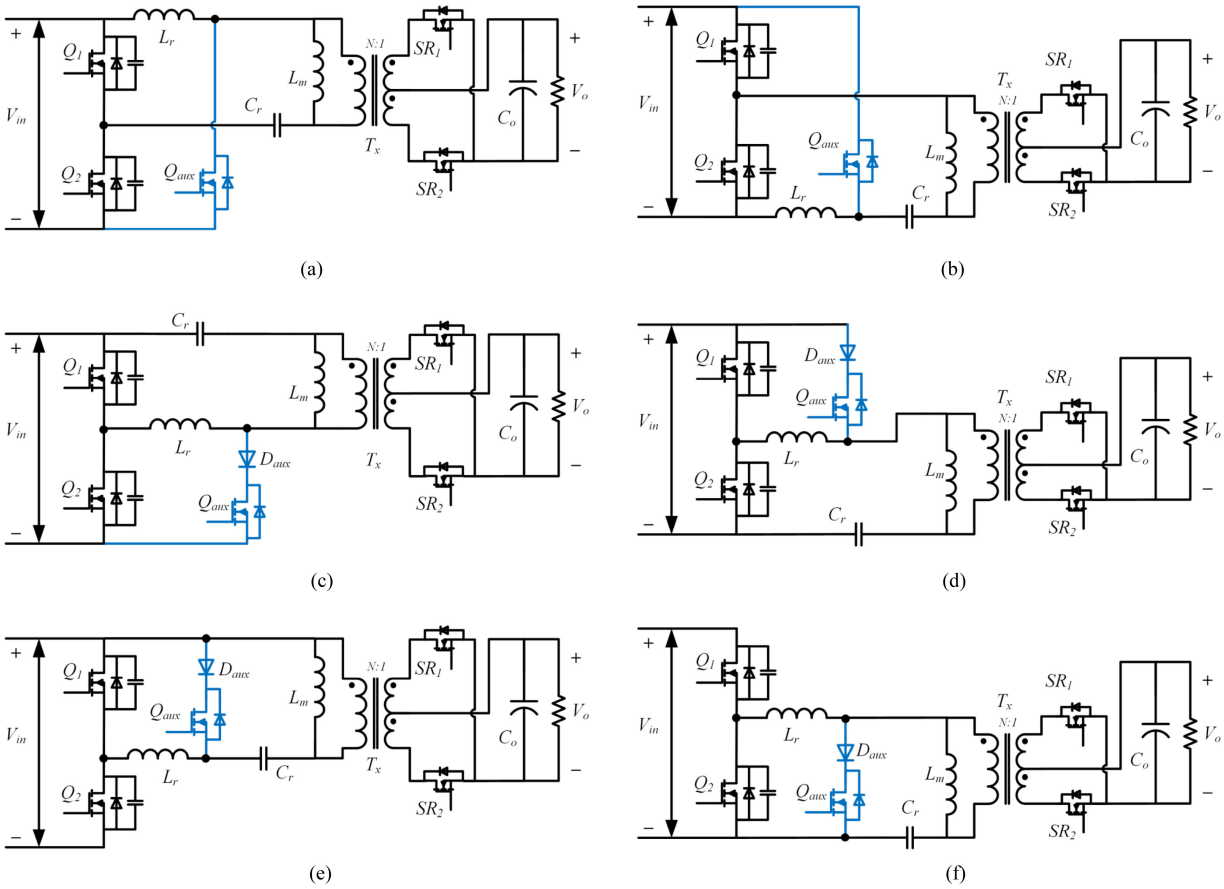

Fig. 12. Topologies of the sLLC converter family for hold-up operation.

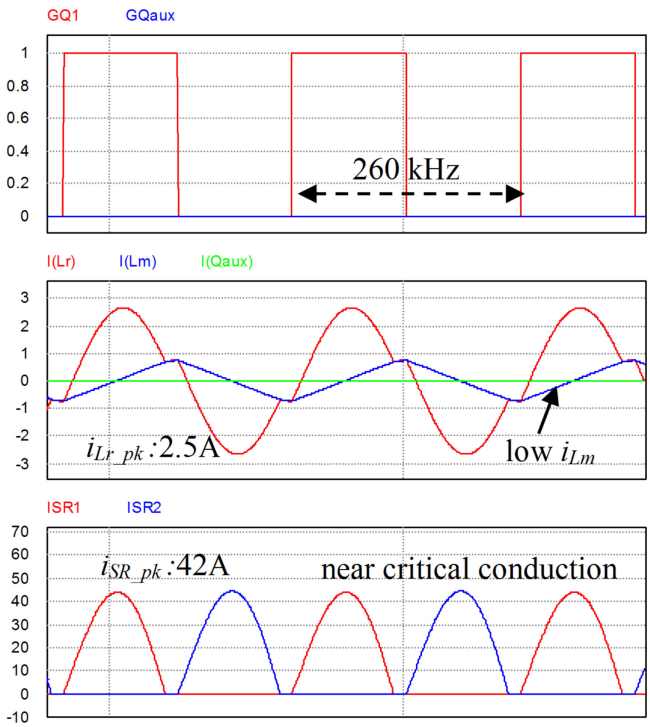

Fig. 13. PSIM simulation of topology #6 for 400 $V_{\rm in}$, 12-V/ 25-A output, f_s = 260 kHz, $D = 0$.

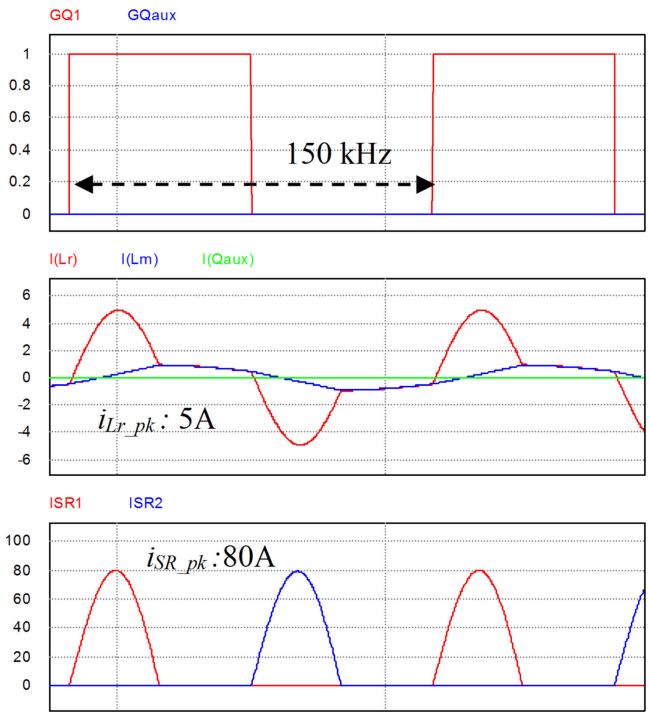

Fig. 14. PSIM simulation of topology #6 for 310 $V_{\rm in}$, 12-V/ 25-A output, f_s = 150 kHz, $D = 0$.

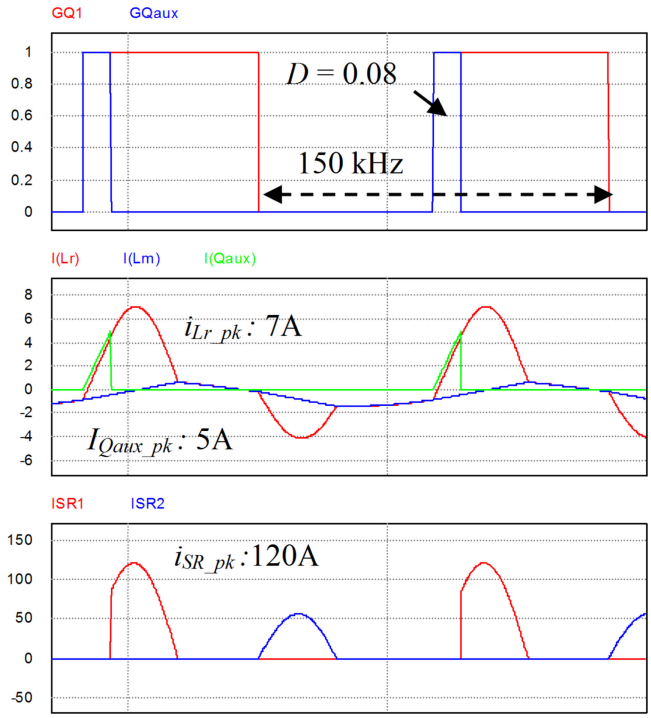

Fig. 15. PSIM simulation of topology #6 for 250 $V_{\rm in}$, 12-V/ 25-A output, f_s = 150 kHz, D = 0.08.

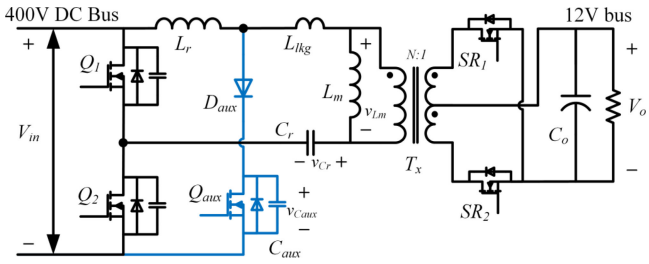

Fig. 16. Circuit diagram for prototype with leakage inductor.

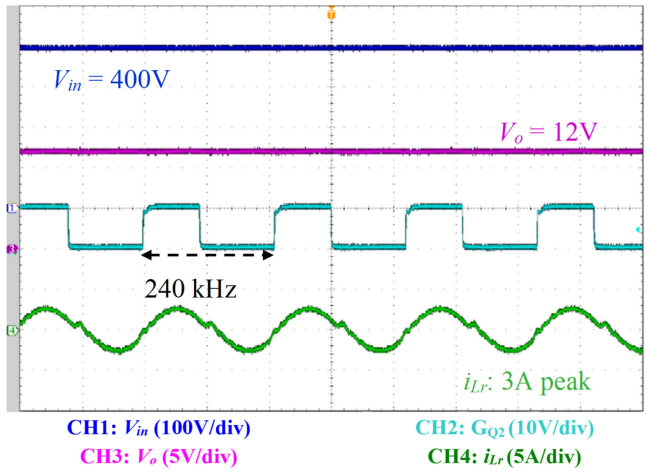

Fig. 17. 400-V input 12-V/25-A full-load steady-state waveform.

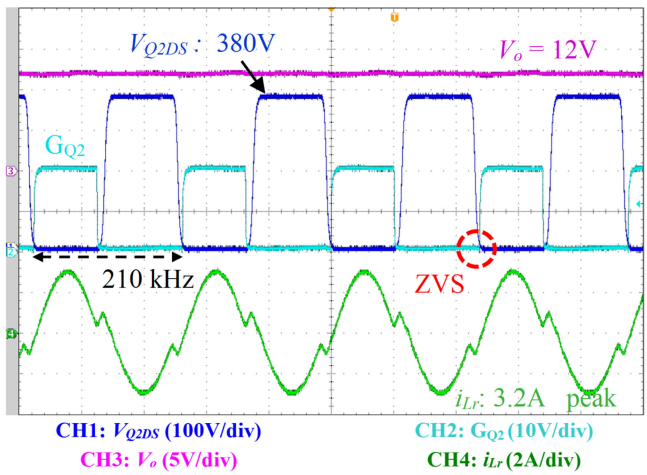

Fig. 18. 380-V input 12-V/25-A full-load steady-state waveform.

In Fig. 14, the input voltage is 310 V. The switching frequency is 150 kHz, at which the HB switches achieves critical ZVS. Thus, this is the lower bound of FM. Further reducing the switching frequency will reduce the output voltage.

In Fig. 15, the input voltage is 250 V. HB switching frequency remains at 150 kHz, and the duty cycle for the auxiliary switch is 0.08.

In this section, the proposed sLLC converter family is introduced. As supplement, sLLC topology #6 operation principle is briefly analyzed. Normal 400-V input operation, 310-V input with minimum switching frequency operation, and 250-V input with auxiliary switch operation are simulated in PSIM.

VI. Experimental Results

A 250–400-V input 12-V/300-W output prototype was built to verify feasibility and advantages of the proposed sLLC converter family and its hold-up ability. The detailed design requirement and power train parameters are given in Table I. The prototype is based on sLLC topology #1. In practice, the leakage inductor of the transformer is inevitable. When the auxiliary switch $Q_{\rm aux}$ is turned OFF, there will be a voltage spike across parasitic capacitor, i.e., $Q_{\rm aux}$. To avoid damage of $Q_{\rm aux}$, in this experiment, as shown in Fig. 16, $C_{\rm aux}$ is added to absorb the voltage spike, and $D_{\rm aux}$ is added to prevent $C_{\rm aux}$ from resonating during the normal operation. It should be noted that the impact of the leakage inductor can be neglected for either low leakage inductance case or low load power case.

Fig. 17 shows the steady-state waveforms of the s*LLC* converter under 300-W full load at 400-V input voltage. The switching frequency is 240 kHz. It is lower than the designed resonant frequency due to the impact of the leakage inductor. The peak value of the resonant current is 3 A.

The resonant current waveform appears a little of asymmetry on 400-V case, because operating near the resonant frequency makes the resonant tank sensitive to the unavoidable mismatch of positive and negative loop impedance. This side effect will be rapidly minimized once the switching frequency deviates from the resonant frequency. Fig. 18 shows the waveform of 380-V input operation. As can be observed, the resonant current waveform becomes quite symmetrical with 210-kHz switching frequency at 380-V input.

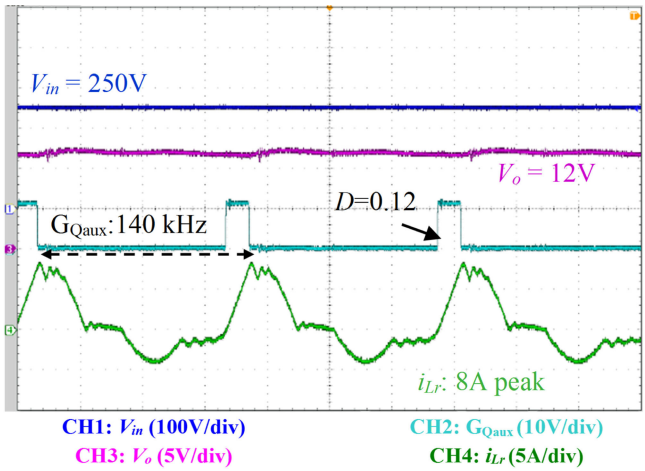

Fig. 19. 250-V input 12-V/25-A full-load steady-state waveform.

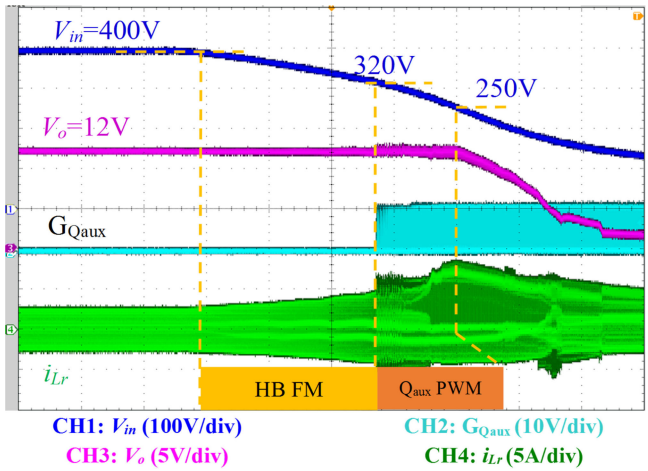

Fig. 21. 12-V/25-A full-load dynamic waveform.

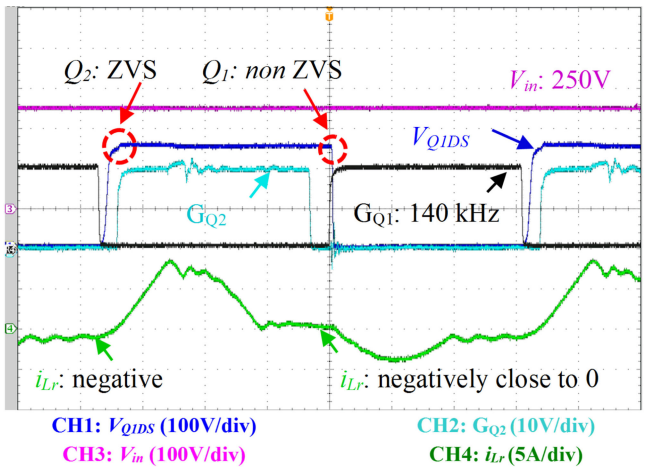

Fig. 20. HB switches ZVS condition at 250-V input 25-A full load.

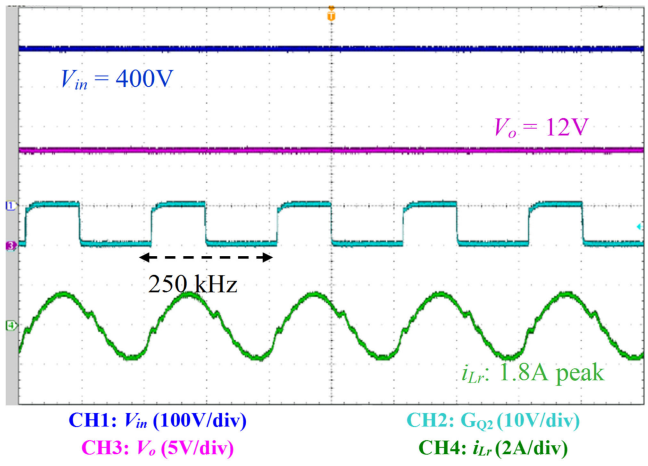

Fig. 22. 400-V input 12-V/15-A 60% load steady-state waveform.

In server and date center application, 380 V is another important input voltage level except for 400 V. The 400-V bus voltage could fluctuate to 380 V, if 5% line frequency ripple from the front PFC stage is allowed. As a fundamental requirement, the *LLC* converter needs to achieve ZVS for the primary switches for 380–400 V. Within this range, the magnetizing current should be properly large to fully discharge the junction capacitors during the switching intervals. As could be observed in Fig. 18, critical ZVS is achieved for Q_1 and Q_2. Below 380 V until 320 V, the resonant tank is still inductive but the junction capacitors are only partly discharged.

Fig. 19 shows the steady-state waveforms of the sLLC converter under 300-W full load at 250-V input voltage. The switching frequency is 140 kHz, which is close to the designed. The duty cycle of the auxiliary switch is around 0.12, which is slightly larger than the simulation results at 0.08, due to the impact of power train losses. The peak value of the inductor current is 8 A. It should be noted that this mode of operation is only during hold-up time with around 20- to 50-ms time period and happens only several times a year. Thus, the selection of $Q_{\rm aux}$ should consider the peak current rating, while thermal design can be derated.

Fig. 20 shows the ZVS condition of the HB switches at 250-V input. Channel 1 shows the voltage across the top switch Q_1. As can be observed, Q_1 loses ZVS due to the presence of dc bias of the magnetizing current, while the bottom switch Q_2 is operated in ZVS. While the top switch may lose ZVS operation during the hold-up time, the conduction loss is significant reduced in Q_1, which mitigates the impact of the extra switching loss. As the hold-up period is very short, thermal design could be derated.

Fig. 21 shows the hold-up process under full load. When the input voltage is between 400 and 320 V, the auxiliary switch is off, and FM of HB switches regulates the output voltage. When the input voltage reduces below 320 V, $Q_{\rm aux}$ starts to take over the output voltage regulation. It could be observed that the output voltage does not lose regulation until the input voltage reduces below 250 V.

Fig. 22 shows the steady-state waveforms of the sLLC converter under 12 V/ 15 A 60% load operating at 400-V input voltage. The switching frequency is 250 kHz. The resonant current is close to sinusoidal. The peak value is 1.8 A.

Fig. 23 shows the steady-state waveforms of the sLLC converter under 12 V/ 15 A 60% load operating at 250-V input voltage. HB switches are operating at the minimum frequency

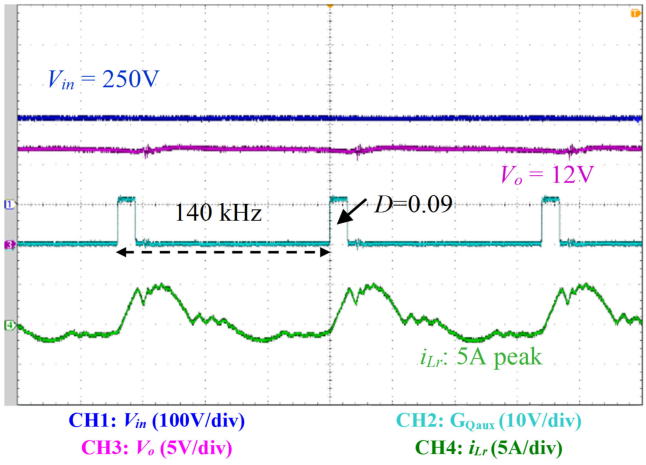

Fig. 23. 250-V input 12-V/15-A 60% load steady-state waveform.

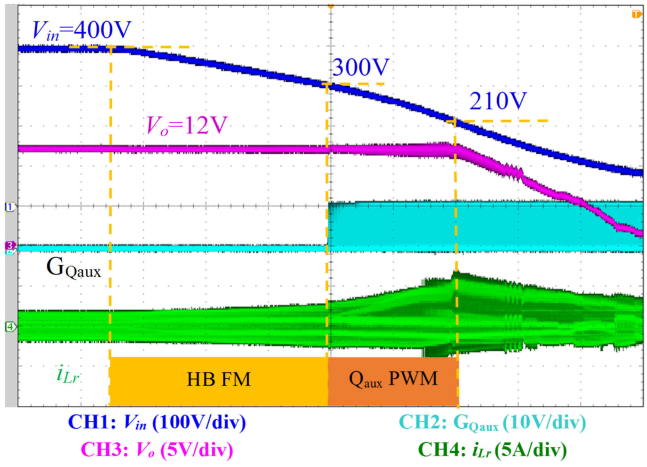

Fig. 24. 12-V/15-A 60% load dynamic waveform.

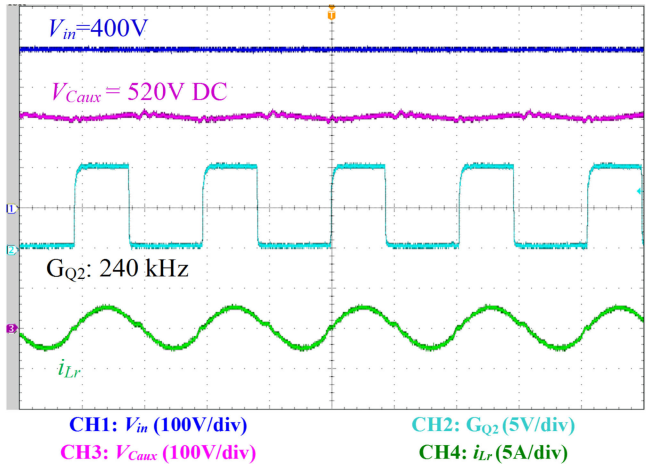

Fig. 25. Voltage stress on the auxiliary switch during steady state.

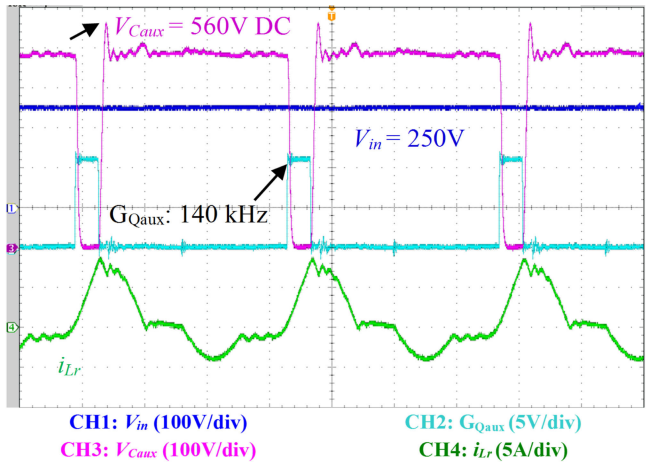

Fig. 26. Voltage stress on auxiliary switch during hold up.

at 140 kHz. The duty cycle of the auxiliary switch is 0.09. The peak value of the inductor current is 5 A. In the simulation, the duty cycle is smaller (at 0.06), as the components are ideal without losses.

Fig. 24 shows the hold-up process under 15 A 60% load. Output voltage can be regulated by FM of HB switches till 300-V input. Between 300 and 210 V, $Q_{\rm aux}$ operates in the PWM mode to hold the output voltage at 12 V.

The waveforms of auxiliary switch voltage stress *vCaux* at steady state are shown in Fig. 25. At steady state, *vCaux* is 520-V dc with 7-V (peak) switching frequency ripple. The ripple results from the resonance of auxiliary parasitic elements and the resonant tank.

Fig. 26 shows the voltage stress on the auxiliary switch *vCaux* at 250-V input. During hold-up time, when the auxiliary switch turns on, the voltage *vCaux* goes to 0. After the auxiliary switch turns off, the accumulated energy in the resonant inductor L_r will be drained by the load.

At the turn off instant, the current gap between the resonant inductor L_r and the leakage inductor $L_{\rm lkg}$ will cause a voltage spike on *Caux*, which peaks at 560 V in the developed prototype with 24 μH L_r and 6 μH $L_{\rm lkg}$ under 250-V input and 25-A full load. Thus, a MOSFET with 650-V voltage rating (IPB65R110CFD) could be used for the auxiliary switch. Such voltage rating is commonly used in the Flyback converter in 220-V ac–dc application. The voltage spike could be reduced with smaller leakage inductor or larger *Caux*. Besides, the overshoot will be less with lighter load.

VII. Conclusion

In this paper, a new family of the HB *LLC* converter with auxiliary switch (sLLC) is proposed to solve the hold-up problems in server and data center power applications. The proposed sLLC converter is suitable for low-voltage application where SR is used. The magnetizing inductor L_m can be integrated into the transformer core to reduce the converter size. Also, L_m can be designed with large value to reduce the circulation loss. During 400-V input, the auxiliary switch will not operate and the circuit operation is the same as that of the conventional *LLC* converter. If input voltage is reduced to a level when the maximum voltage gain is achieved (minimum switching frequency is reached), the auxiliary switch starts to operate at the PWM mode to increase the energy transferred into the resonant inductor in one switching cycle. Thus, the voltage gain is improved, and the

output voltage can be maintained at 12 V. In this paper, detailed operation modes are examined and analyzed. Besides, a simplified circuit operation is proposed, based on which closed-form equations of current and voltage stresses are developed to assist the design of the converter. PSIM simulations are conducted to verify the operation at different input conditions. A 250–400-V input, 300-W prototype has been built to verify the proposed sLLC converter. The experiment results justify the feasibility and effectiveness of topology and analysis.

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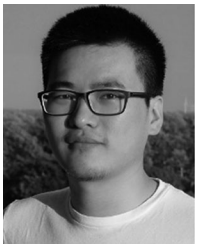

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